Erratum

In [1], regrettably, several author corrections were left out in the final printing, and the authors' photographs were incorrect.

Algorithms 1 and 2 were not indented correctly. The following are the corrected versions of Algorithms 1 and 2.

Algorithm 1 Technology Mapping for Domino Circuits

{Process each node in topological order from inputs to outputs}
for each node n whose inputs have been processed **do**
  for each $\{W, H\}$ configuration of the inputs **do**
    if n is OR **then**
      $\{W_{new}, H_{new}\} = \{W_1 + W_2, max(H_1, H_2)\}$
    end if
    if n is AND **then**
      $\{W_{new}, H_{new}\} = \{max(W_1, W_2), H_1 + H_2\}$
    end if
    if $\{W_{new}, H_{new}\}$ is a valid configuration **then**
      $cost_{new} = cost_1 + cost_2$
    end if
    if $cost_{new}$ is better than the original cost **then**
      update $cost$ for configuration $\{W_{new}, H_{new}\}$
    end if
  end for
  $\{1, 1\}$ = convert configuration with min. cost into a gate
end for

Algorithm 2 Algorithm for Mapping SOI Circuits

for each node n whose inputs have been processed **do**
  if n is OR **then**
    `combine_or(inputs)` ;
  end if
  if n is AND **then**
    `combine_and(inputs)` ;
  end if
  if multiple tuples obtained for the same W, H **then**
    Select tuple with lowest cost
    if costs are equal **then**
      Select tuple with lowest p_{dis}
    end if
  end if
  `create_domino_gate`
end for

`combine_or`
$W = W_{input_1} + W_{input_2}$;
$H = \max(H_{input_1}, H_{input_2})$;
$cost = cost_{input_1} + cost_{input_2}$;
$p_{dis} = p_{dis^{input_1}} + p_{dis^{input_2}}$;
$par_b = true$;

`combine_and`
if $par_{b^{input_1}}$ && $par_{b^{input_2}}$ **then**
  $top = \min(p_{dis^{input_1}}, p_{dis^{input_2}})$;
  $bottom = \max(p_{dis^{input_1}}, p_{dis^{input_2}})$;
else
  top = input with $(par_b == false)$;
end if
$W = \max(W_{top}, W_{bottom})$;
$H = H_{top} + H_{bottom}$;
$total\ dis\ trans. = p_{dis^{top}} + 1$;
$cost = cost_{top} + cost_{bottom} + total\ dis\ trans$;
$p_{dis} = p_{dis^{bottom}}$;
$par_b = par_{b^{bottom}}$;

`create_domino_gate`
Select tuple with lowest cost
Add p-clock transistor, output inverter
    and feedback transistor
if tuple has primary inputs **then**
  Add n-clock transistor
end if

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Also, the caption of Fig. 2 was modified inaccurately. Fig. 2 is shown with its correct caption.

Lastly, the photographs of both authors were incorrect and the last sentence in S. Sapatnekar's biography, which should have been deleted, was inadvertently left in. The following are the authors biographies with the correct photographs and text.

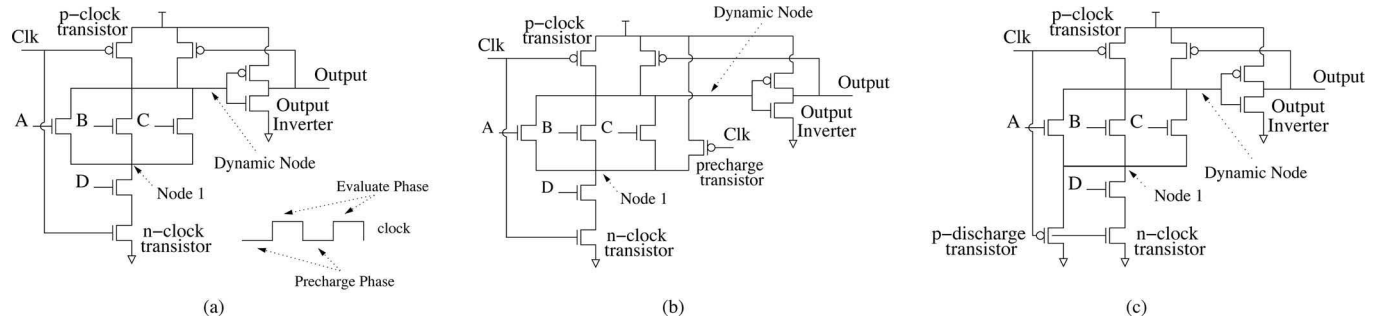

Fig.2. (a) Domino gate structure and modifications applied in (b) bulk CMOS and (c) SOI technologies.

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REFERENCES

[1] S. K. Karandikar and S. S. Sapatnekar, "Technology mapping for SOI domino logic incorporating solutions for the parasitic bipolar effect," *IEEE Trans. VLSI Syst.*, vol. 11, no. 6, pp. 1094–1105, Dec. 2003.